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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/670,620	09/25/2003	Jeffrey C. Swanson	10002929-3	6729

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HEWLETT-PACKARD COMPANY
Intellectual Property Administration
P. O. Box 272400
Fort Collins, CO 80527-2400

EXAMINER	
MASKULINSKI, MICHAEL C	

ART UNIT	PAPER NUMBER
2113	

DATE MAILED: 07/14/2006

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)	
	10/670,620	SWANSON ET AL.	
	Examiner	Art Unit	
	Michael C. Maskulinski	2113	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *16 May 2006*.

2a)☒ This action is **FINAL**. 2b)☐ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-21* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☒ Claim(s) *17,18 and 20* is/are allowed.

6)☒ Claim(s) *1-16 and 19* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☐ The drawing(s) filed on _____ is/are: a)☐ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☐ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date _____.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____ .
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: _____.

Final Office Action

Double Patenting

1. The nonstatutory double patenting rejection is based on a judicially created doctrine grounded in public policy (a policy reflected in the statute) so as to prevent the unjustified or improper timewise extension of the "right to exclude" granted by a patent and to prevent possible harassment by multiple assignees. A nonstatutory obviousness-type double patenting rejection is appropriate where the conflicting claims are not identical, but at least one examined application claim is not patentably distinct from the reference claim(s) because the examined application claim is either anticipated by, or would have been obvious over, the reference claim(s). See, e.g., In re Berg, 140 F.3d 1428, 46 USPQ2d 1226 (Fed. Cir. 1998); In re Goodman, 11 F.3d 1046, 29 USPQ2d 2010 (Fed. Cir. 1993); In re Longi, 759 F.2d 887, 225 USPQ 645 (Fed. Cir. 1985); In re Van Ornum, 686 F.2d 937, 214 USPQ 761 (CCPA 1982); In re Vogel, 422 F.2d 438, 164 USPQ 619 (CCPA 1970); and In re Thorington, 418 F.2d 528, 163 USPQ 644 (CCPA 1969).

A timely filed terminal disclaimer in compliance with 37 CFR 1.321(c) or 1.321(d) may be used to overcome an actual or provisional rejection based on a nonstatutory double patenting ground provided the conflicting application or patent either is shown to be commonly owned with this application, or claims an invention made as a result of activities undertaken within the scope of a joint research agreement.

Effective January 1, 1994, a registered attorney or agent of record may sign a terminal disclaimer. A terminal disclaimer signed by the assignee must fully comply with 37 CFR 3.73(b).

2. Claims 1-21 are rejected on the ground of nonstatutory obviousness-type double patenting as being unpatentable over claims 1-17 of U.S. Patent No. 6,662,313 B1. Although the conflicting claims are not identical, they are not patentably distinct from each other because of the following.

Referring to claim 1, claim 1 of U.S. Patent 6,662,313 B1 discloses circuitry for providing external access to signals that are internal to an integrated circuit, said circuitry comprising: a network comprising a plurality of multiplexers physically distributed throughout the integrated circuit, each of said multiplexers having its inputs coupled to a nearby set of nodes within the integrated circuit; and a trigger event

generator receiving a first N bits of sampled data from said network, said trigger event generator including a definable mask and selectively performing a boolean operation on said sampled data based on said mask to provide a trigger event. Although the conflicting claims are not identical, they are not patentably distinct from each other because claim 1 of U.S. Patent 6,662,313 B1 includes all of the limitations in claim 1 of the instant application. With regard to the additional limitations in claim 1 of U.S. Patent 6,662,313 B1, which are not included in claim 1 of the instant application, the omission of these limitations in claim 1 of the instant application is an obvious expedient since the remaining limitations in claim 1 of U.S. Patent 6,662,313 B1 perform the same function as the limitations in claims 12, 19, and 20 of the instant application (*In re Karlson*, 136 USPQ 184 (CCPA 1963)).

Referring to claim 2, claim 2 of U.S. Patent 6,662,313 B1 discloses wherein said trigger event generator further comprises a switch for selectively providing, as said trigger event, one of (i) a result of said boolean operation on said sampled data, (ii) a performance counter event signal, and (iii) an externally applied trigger signal.

Referring to claim 3, claim 3 of U.S. Patent 6,662,313 B1 discloses a counter providing an intermediate trigger in response to a predetermined number of said trigger events.

Referring to claim 4, claim 4 of U.S. Patent 6,662,313 B1 discloses a trigger delay providing a sample command a predetermined number of cycles following said intermediate trigger.

Referring to claim 5, claim 5 of U.S. Patent 6,662,313 B1 discloses said predetermined number of cycles represent respective operating cycles of the integrated circuit.

Referring to claim 6, claim 6 of U.S. Patent 6,662,313 B1 discloses wherein said predetermined number of cycles represent respective machine clock cycles.

Referring to claim 7, claim 7 of U.S. Patent 6,662,313 B1 discloses a programmable register storing a value corresponding to said predetermined number of cycles.

Referring to claim 8, claim 8 of U.S. Patent 6,662,313 B1 discloses wherein said programmable register selectively increments said value corresponding to said predetermined number of cycles by a predetermined number of said cycles.

Referring to claim 9, claim 9 of U.S. Patent 6,662,313 B1 discloses a sampling circuit responsive to said sample command to identify target data.

Referring to claim 10, claim 10 of U.S. Patent 6,662,313 B1 discloses a trigger delay providing a sample command a predetermined number of cycles following said trigger event.

Referring to claim 11, claim 11 of U.S. Patent 6,662,313 B1 wherein the sampling circuit is responsive to said sample command to identify target data.

Referring to claim 12, claim 1 of U.S. Patent 6,662,313 B1 discloses a sampling circuit responsive to said trigger event to identify target data.

Referring to claim 13, claim 12 of U.S. Patent 6,662,313 B1 discloses said target data comprises said first N bits of sampled data supplied by said network.

Referring to claim 14, claim 13 of U.S. Patent 6,662,313 B1 discloses wherein said target data consists of a second N bits of sampled data supplied by said network.

Referring to claim 15 claims 1 and 14 of U.S. Patent 6,662,313 B1 discloses a FIFO storage array (a memory) that stores at least a portion of the sampled data wherein said sampling circuit includes the FIFO array and the portion of the sampled data is said target data.

Referring to claim 16, claim 15 of U.S. Patent 6,662,313 B1 wherein said sampling circuit includes switching circuitry configured to selectively provide a predetermined portion of said target data.

Referring to claim 17, claim 16 of U.S. Patent 6,662,313 B1 discloses wherein said predetermined portion of said target data is N/M bits wide where N/M is a positive integer.

Referring to claim 18, claim 17 of U.S. Patent 6,662,313 B1 discloses wherein said sampling circuit includes multiplexing circuitry configured to combine M of said portions of said target data into a data unit N bits wide.

Referring to claim 19, claim 1 of U.S. Patent 6,662,313 B1 discloses wherein said sampling circuit includes the FIFO storage array.

Referring to claim 20, claim 1 of U.S. Patent 6,662,313 B1 discloses the FIFO storage that is N/M bits wide where N/M is a positive integer.

Referring to claim 21, claim 1 of U.S. Patent 6,662,313 B1 discloses a FIFO storage array that stores at least a portion of the sampled data.

Claim Rejections - 35 USC § 112

3. In view of the recent amendments, the rejection of claim 19, under 35 U.S.C. 112, second paragraph, has been withdrawn.

Claim Rejections - 35 USC § 102

4. The text of those sections of Title 35, U.S. Code not included in this action can be found in a prior Office action.

5. Claims 1-3, 12-16, and 19 are rejected under 35 U.S.C. 102(b) as being anticipated by Ranson et al., U.S. Patent 5,867,644.

Referring to claim 1:

a. In column 28, lines 57-64, Ranson et al. disclose that various 16:1 multiplexers are physically located at various remote locations around the microprocessor. Each has its inputs coupled to a set of test nodes (a network comprising a plurality of multiplexers physically distributed throughout the integrated circuit, each of said multiplexers having its inputs coupled to a nearby set of nodes within the integrated circuit).

b. In column 15, lines 44-67 continued in column 16, lines 1-5, Ranson et al. disclose that the four bits of present state bus are provided to one of the inputs of comparator so that they may be compared with the contents of storage element, which specifies the present state during which entry will become active (a trigger event generator receiving a first N bits of sampled data from said network). The four bits that are output from the comparator are ANDed together at AND gate,

yielding a one-bit match result for present state. Similarly, the contents of storage element 1202 are compared with the eleven bits of state machine input bus by the comparator. An OR gate is used to mask the output bits of the comparator with the contents of the storage element. The results of this masking operation are ANDed together, resulting in a match result for the state machine input bus (said trigger event generator including a definable mask and selectively performing a Boolean operation on said sampled data based on said mask to provide a trigger event).

c. In Figure 4 and in column 13, lines 38-67 continued in column 14, lines 1-62, Ranson et al. teach a FIFO storage array that stores at least a portion of the sampled data.

Referring to claim 2:

a. In column 15, lines 44-57, Ranson et al. disclose the four bits that are output from the comparator are ANDed together at AND gate, yielding a one-bit match result for present state (a result of said Boolean operation on said sampled data).

b. In column 3, lines 55-58, Ranson et al. disclose that the outputs from the counters may also be used as state machine inputs, so that one event may be defined as a function of a different event having occurred a certain number of times (a performance counter event signal).

c. In the Abstract, Ranson et al. disclose that the output devices also include circuitry for generating internal and external triggers (an externally applied trigger signal).

Referring to claim 3, in column 3, lines 55-58, Ranson et al. disclose that the outputs from the counters may also be used as state machine inputs, so that one event may be defined as a function of a different event having occurred a certain number of times (a counter providing an intermediate trigger in response to a predetermined number of said trigger events).

Referring to claim 12, in column 3, lines 47-49, Ranson et al. disclose a diagnostics retrieval system that initiates operation of the integrated circuit and monitors the external pulse signal (a sampling circuit responsive to said trigger command to identify target data).

Referring to claims 13 and 14, in columns 16-26, Ranson et al. disclose sample-on-the-fly circuitry that latches the state of the test nodes 0-n whenever a control signal is asserted (a first and second N bits of sampled data supplied by said network).

Referring to claim 15, in Figure 4, Ranson et al. disclose remote registers for storing the data (said sampling circuit includes a memory storing said target data).

Referring to claim 16, in column 11, lines 16-26, Ranson et al. disclose sample-on-the-fly circuitry that latches the state of the test nodes 0-n whenever a control signal is asserted (switching circuitry configured to selectively provide a predetermined portion of said target data).

Referring to claim 19, in Figure 4, Ranson et al. disclose a storage array in which the bits are shifted serially through the remote registers (wherein said sampling circuit includes a FIFO storage array).

Claim Rejections - 35 USC § 103

6. The text of those sections of Title 35, U.S. Code not included in this action can be found in a prior Office action.

7. Claims 4-11 are rejected under 35 U.S.C. 103(a) as being unpatentable over Ranson et al., U.S. Patent 5,867,644 as applied to claim 1 above, and further in view of Tobin et al., U.S. Patent 5,771,240.

Referring to claims 4 and 10, in column 3, lines 55-58, Ranson et al. teach an intermediate trigger signal. However, Ranson et al. don't explicitly disclose a trigger delay providing a sample command a predetermined number of cycles following said intermediate trigger. In column 4, lines 16-31, Tobin et al. disclose a programmable countdown timer that is configured to keep track of the number of clock cycles which pass once its input trigger capture signal is received, and produces a countdown timer enable signal when the number of clock cycles which have passed equals the programmed clock cycle count. It would have been obvious to one of ordinary skill at the time of the invention to include the countdown timer of Tobin et al. into the system of Ranson et al. A person of ordinary skill in the art would have been motivated to make the modification because *the ability of the debug trigger apparatus to precisely control the signaling delay of the trigger capture signal is critical to allowing the test system to*

iteratively retrieve continuous yet discrete test node signal events from the integrated circuit in order to form a useful trace of events for use in debugging problems and failures of the integrated circuit (see Tobin et al.: column 4, lines 25-31).

Referring to claim 5, in column 4, lines 16-18, Tobin et al. disclose the programmable countdown timer may be set to countdown a programmed number of clock cycles before signaling a trigger capture signal (said predetermined number of cycles represent respective operating cycles of the integrated circuit).

Referring to claim 6, in column 4, lines 16-18, Tobin et al. disclose the programmable countdown timer may be set to countdown a programmed number of clock cycles before signaling a trigger capture signal (said predetermined number of cycles represent respective machine clock cycles).

Referring to claim 7, in Figure 8, Tobin et al. disclose a register for the countdown timer (a programmable register storing a value corresponding to said predetermined number of cycles).

Referring to claim 8, in column 3, lines 47-58, Tobin et al. disclose that when an external pulse signal is received, the diagnostics retrieval system may then reset the integrated circuit, reprogram the trigger condition, and set the programmed delay to a second delay value which is a known increment greater than the first delay value (said programmable register selectively increments said value corresponding to said predetermined number of cycles by a predetermined number of said cycles).

Referring to claim 9, in column 3, lines 47-49, Ranson et al. disclose a diagnostics retrieval system that initiates operation of the integrated circuit and monitors

the external pulse signal (a sampling circuit responsive to said sample command to identify target data).

Referring to claim 11, in column 3, lines 47-49, Ranson et al. disclose a diagnostics retrieval system that initiates operation of the integrated circuit and monitors the external pulse signal (a sampling circuit responsive to said sample command to identify target data).

Allowable Subject Matter

8. Claims 17, 18, and 20 are allowed.

9. The following is a statement of reasons for the indication of allowable subject matter.

Referring to claim 17, the prior art does not teach or reasonably suggest wherein said predetermined portion of said target data is N/M bits wide where N/M is a positive integer.

Referring to claim 20, the prior art does not teach or reasonably suggest wherein said FIFO storage array is N/M bits wide where N/M is a positive integer.

Response to Arguments

10. Applicant's arguments filed May 16, 2006 have been fully considered but they are not persuasive.

11. On page 7, under section **VI Rejections Under 35 U.S.C. § 102**, the Applicant argues, "The Office Action cites Ranson at figure 4 and the passage at column 13, line

38 through column 14, line 62 to teach the feature. However, these portions of Ranson do not teach the feature because they do not teach a FIFO storage array. For instance, figure 4 shows a 'staging register' and 'remote registers,' but does not teach that any of those registers are FIFOs. A register, by itself, is not enough to teach a FIFO, and figure 4 is not sufficient to teach the feature in as complete detail as contained in the claim." The Examiner disagrees. A more careful reading of Ranson et al. would show many examples of why the registers of Ranson et al. are FIFO registers. For example, the serial data in Figure 4 is shown to be shifted through the Remote Registers in a FIFO manner. This is further supported in column 13, lines 39-67 continued in column 14, lines 1-12, where Ranson et al. disclose loading data into a register and then serially shifting it out header first to another register. Since headers are always at the beginning of data, this data is shifted out in a FIFO manner.

12. On page 8, under section **VII Rejections Under 35 U.S.C. § 103**, the Applicant does not argue the motivation to combine the references or the combination of the references. Therefore, the Applicant concedes that the combination of Ranson in view of Tobin is proper.

Conclusion

13. **THIS ACTION IS MADE FINAL.** Applicant is reminded of the extension of time policy as set forth in 37 CFR 1.136(a).

A shortened statutory period for reply to this final action is set to expire THREE MONTHS from the mailing date of this action. In the event a first reply is filed within TWO MONTHS of the mailing date of this final action and the advisory action is not

mailed until after the end of the THREE-MONTH shortened statutory period, then the shortened statutory period will expire on the date the advisory action is mailed, and any extension fee pursuant to 37 CFR 1.136(a) will be calculated from the mailing date of the advisory action. In no event, however, will the statutory period for reply expire later than SIX MONTHS from the mailing date of this final action.

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Michael C. Maskulinski whose telephone number is (571) 272-3649. The examiner can normally be reached on Monday-Friday 9:30-6:00.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Robert W. Beausoliel can be reached on (571) 272-3645. The fax phone number for the organization where this application or proceeding is assigned is 571-273-8300.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free). If you would like assistance from a USPTO Customer Service Representative or access to the automated information system, call 800-786-9199 (IN USA OR CANADA) or 571-272-1000.

MM